

11 GHz SiGe Circuits for Ultra Wideband Radar

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ABSTRACT: Transmitter and receiver circuits operating at 11 GHz system clock rate are described. These circuits, fabricated in a 0.8 μm SiGe-HBT technology, are the key elements of a radar head using a new ultra wideband principle.

Introduction

Ultra wideband (UWB) radar and related measurements are of great importance for a vast number of applications such as surface penetrating radar, surveillance and emergency equipment, medical instrumentation, non-destructive testing in civil engineering, industrial sensors, microwave imaging etc. The silicon germanium (SiGe) technology allows the realisation of high frequency integrated circuits with high yield and high reliability. The SiGe RF circuits presented in this paper are the key elements of a radar head using a new UWB principle [1].

is captured by a track and hold (T&H) circuit operating in an undersampling mode so that low cost ADCs and acquisition memories can be applied. Since for every chip of the MLBS only one sample of the measurement signal is needed, the acquisition clock may be directly derived from the RF master clock by a binary divider.

SiGe HBT Technology

For fabrication of the RF circuits we used the 0.8 μm SiGe HBT technology of the IHP in Frankfurt (Oder). In this low-cost process, the HBTs are fabricated as single polysilicon devices with implanted, epi-free collectors (for more details see [2,3]).

The technology offers npn transistors with emitter areas in the range 1 - 70 μm^2 and a library with passive elements: Resistor types of 200 Ohm per square (polysilicon) and 10 Ohm per square (silicide), MIM capacitors with 1 fF/ μm^2 , varicaps and inductors (L between 0.5 and 13.5 nH). The HBT parameters of this technology are summarised in Table 1.

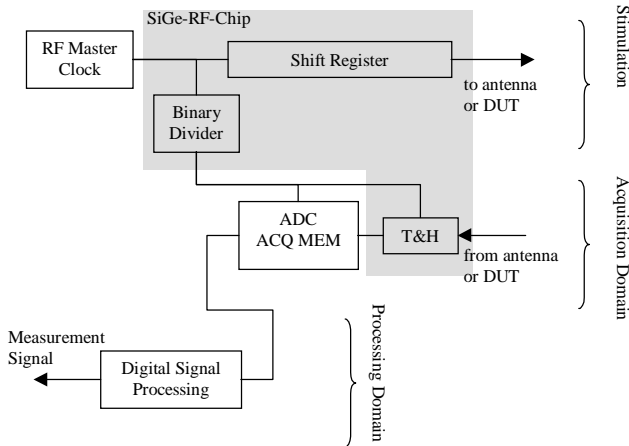


Fig. 1: Basic structure of the UWB head

Figure 1 shows the basic structure of the UWB head. A single tone RF generator (master clock) pushes a digital shift register. If this shift register disposes of appropriate feedbacks, it provides a so-called Maximum Length Binary Sequence (MLBS) at its output. This signal serves as a radar test signal. It is periodic and has a very large bandwidth which is determined by the maximum toggle frequency of the shift register. The bandwidth usable for the measurement is $0 \dots f_c/2$, in which f_c is the master clock rate. One period of the MLBS contains $2^n - 1$ pseudo-randomly distributed chips, in which n is the number of stages in the shift register. The actual measurement signal

Parameter	Value
f_T	45 GHz @ $V_{CE} = 2$ V
f_{max}	50 GHz @ $V_{CE} = 2$ V
Ring oscillator delay	22 .. 25 ps, $F_i/F_o = 1$, $\Delta V = 200$ mV
β_{max}	80 - 150
Early voltage V_A	40 V, $V_{BE} = 0.6$ V, $V_{CB} = 0$ V
BV_{CEO}	2.7 V
NF_{min}	< 3 dB @ 10 GHz

Table 1: Typical HBT parameters

It has recently been demonstrated that the performance of this SiGe HBT technology can be significantly improved by the addition of carbon in the base [4]. The modular integration of this SiGe:C HBT in a deep sub-micron CMOS process was presented by Ehwald et al. [5].

SiGe Bipolar Logic

The circuit diagram of a current mode logic (CML) AND/OR cell with SiGe HBTs is shown in Fig. 2. The logic cells and the whole MLBS generator circuit are fully differential designed in order to reduce time jitter and interference. The internal differential voltage swing is about 400

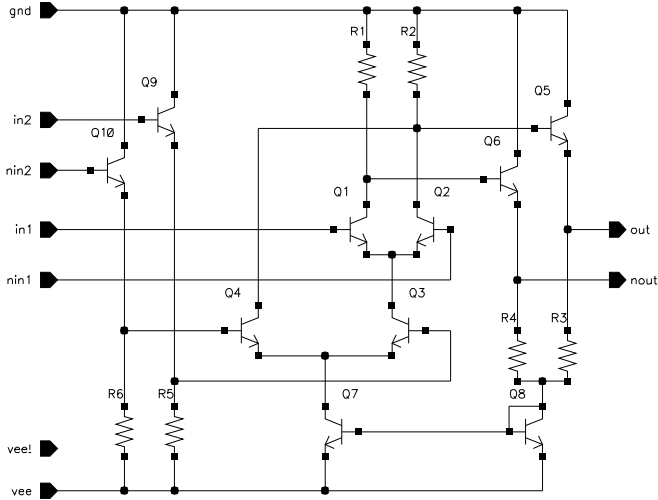


Fig. 2: Differential SiGe bipolar logic cell

mV_{pp} . This allows a maximum operational speed > 11 GHz (found by circuit simulation). Logic combinations of more than 2 inputs may be realised by the introduction of additional current switch levels. The number of current switch levels is limited by the operating voltage with regard to the maximum tolerable power dissipation of the circuit. Up to 3 current switch levels are used in the UWB circuits.

The Transmitter Circuit

The core elements of the transmitter circuit are a 9-stage MLBS generator and a frequency divider with a controllable binary divider factor. The MLBS generator circuit, which consists of a linear feedback shift register with 9 master-slave flip-flop stages, is shown in Fig. 3. To realise the feedback, the first flip-flop stage contains an embedded XOR gate. The embedding of the logic combination reduces the propagation delay of this stage and increases the maximum clock rate of the circuit.

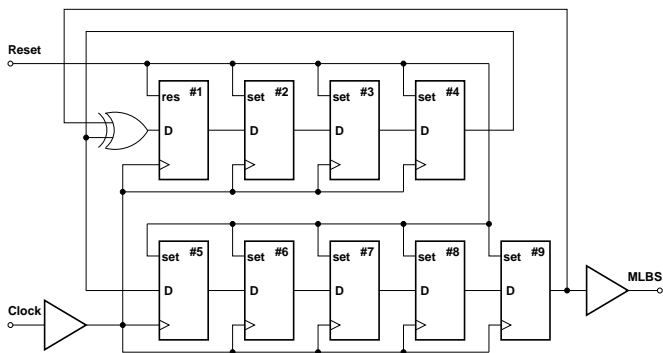


Fig. 3: Circuit diagram of the MLBS generator

We realised each individual flip-flop cell with a 2-level current switch (3 levels in the case of embedded logic) technique, similar to the logic cell described above. The simulation shows the capability to drive such flip-flops built of integrated SiGe HBTs with clock rates of more than 11 GHz.

The whole transmitter circuit fits on a single chip with a size of $2 \times 2 \text{ mm}^2$. Figure 4 shows the photo-micrograph of the transmitter chip.

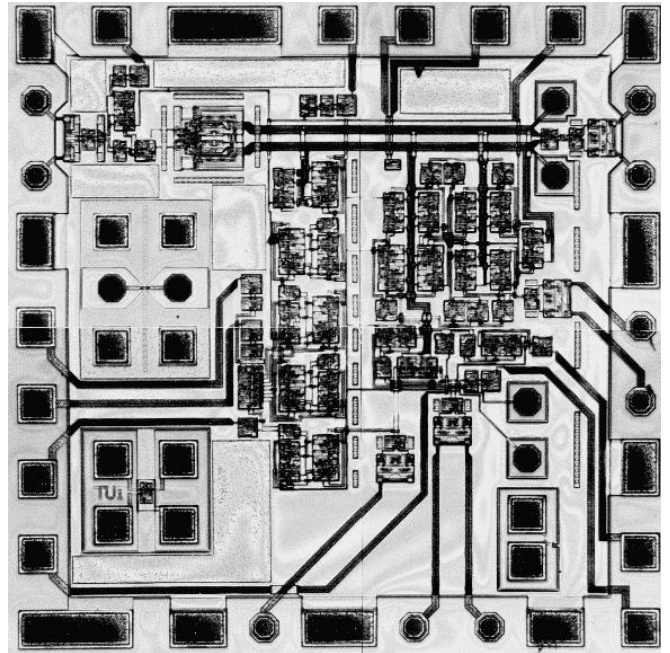


Fig. 4: Photo-micrograph of the SiGe transmitter IC; the chip size is $2 \times 2 \text{ mm}^2$

The flip-flop cells of the MLBS generator are placed in two rows with opposite shift direction in order to reduce the wire length for better high speed performance. The second main block on the chip is the clock divider. Binary divider factors from 2^7 to 2^{10} are externally controllable. The divider output and some other control signals are synchronised to the external system clock by a separate synchronisation unit. The internal clock is distributed by a low power dissipating clock driver with clock recovery capability. All RF inputs are terminated on chip (100Ω differential / 50Ω single ended). The RF inputs and outputs are fully differential. The RF outputs are capable to drive 800 mV_{pp} into a 100Ω load (symmetrical) or $2 \times 400 \text{ mV}_{pp}$ into a 50Ω load (single ended). All other control inputs and outputs are designed to be compatible to TLL logic.

The transmitter circuit is operated by a single 5 V power supply. We measured a power dissipation of less than 2 W . An on-chip heat sensor is available because self heating of the transmitter chip may become a problem in practical use.

The Receiver Circuit

The core of the receiver is the bipolar differential track & hold (T&H) circuit, which is shown in Fig. 5. The operational principle is as follows: In track mode the circuit behaves like a linear unity gain amplifier, which consists of three emitter follower stages. While the current switch transistors $Q3/Q3'$ are switched on, the currents $I1/I1'$ drive the transistors $Q1/Q1'$ to operate in normal amplification mode. As the output impedance of the emitter followers $Q1/Q1'$ is low, the hold capacitors CH/CH' may be driven up to the

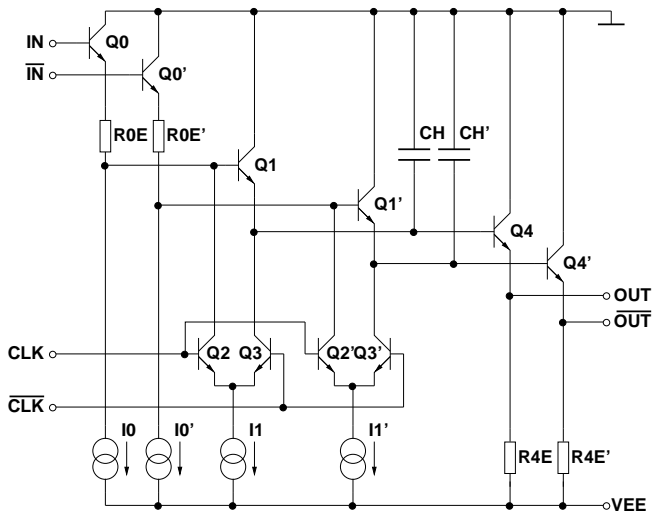


Fig. 5: Track & hold receiver core circuit

full operational bandwidth of the receiver (the receiver bandwidth must be 50 % of the master clock rate).

If the T&H clock turns to high, the current switch transistors Q2/Q2' are switched on whereas Q3/Q3' are switched off. The currents I1/I1' are superimposed on the currents I0/I0' driving the input emitter follower stage. As a result, the voltage drop over the emitter resistors R0E/R0E' rises. While Q3/Q3' are switched off, the emitter potentials of Q1/Q1' are held on their values at the time of the clock rising edge by CH/CH'. If the additional voltage drop across R0E/R0E' is high enough (> approx. 200 mV), the transistors Q1/Q1' are safely switched off and the circuit remains in hold mode. The emitter followers Q4/Q4' decouple the hold capacitors from the low impedance output. The input leakage current of Q4/Q4' determines the maximum hold time of the circuit. A hold time > 20 ns may be obtained by a hold capacitance of about 400 fF. These capacitors can easily be integrated on chip since the SiGe technology provides MIM capacitors with a specific capacitance of 1 fF/ μm^2 .

The receiver layout has been designed with special attention to maximum RF decoupling between input and output. The chip size of the receiver IC is 2 x 1 mm². The operating voltage is 6 V from a single power supply. The total power dissipation does not exceed 350 mW.

Experimental Results

To perform the RF measurements the transmitter and receiver ICs were bond-wire mounted on thick film Al₂O₃ ceramic carriers suitable for test packages with SMA connectors. All RF lines on the ceramic carriers are 50 Ω matched micro strip lines with length compensation for each differential pair. The lengths of the bond-wires connecting the RF pads were kept as short as possible in order to reduce parasitic inductances. Heat dissipation of the ceramic carrier in conjunction with the brass test package keeps the chip temperature of the transmitter below 100 $^{\circ}\text{C}$ under operational conditions without active cooling.

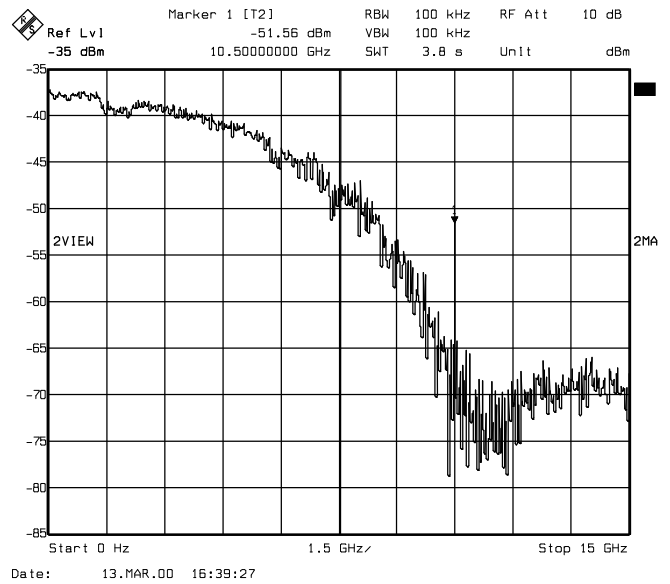


Fig. 6: MLBS power spectrum at 10.5 GHz master clock rate

The master clock was driven by a conventional RF generator with an external balun to adapt the single ended generator output to the differential transmitter clock input.

The correct operation of the divider unit has been verified up to 12 GHz master clock rate. A spectrum analyser was used to test the MLBS generator. Figure 6 shows the measured MLBS power spectrum at 10.5 GHz master clock rate. It shows the $\text{sinc}^2(f/f_c)$ -shape (superimposed by the output driver frequency response) which is typical for an MLBS. The output driver bandwidth was derived from rise and fall time measurements of the clock divider output signal using a 50 GHz transient analyser. We found a rise time of 36 ps and a fall time of 42 ps (single ended) corresponding to approx. 10 GHz driver bandwidth.

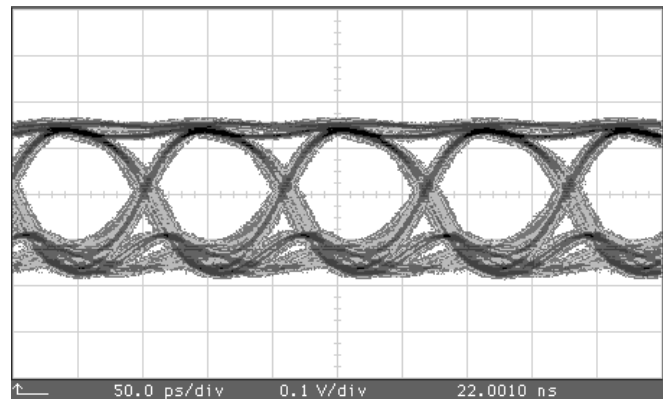


Fig. 7: MLBS output eye pattern at 9.4 GHz master clock rate (single ended)

The MLBS output eye pattern at 9.4 GHz master clock frequency is shown in Fig. 7. It shows wide-open eyes with a peak-to-peak output voltage swing of about 300 mV single ended ($R_{\text{load}} = 50 \Omega$).

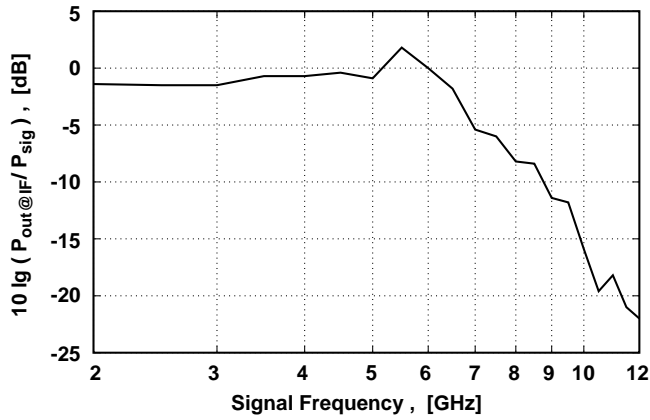


Fig. 8: Measured receiver frequency response

The receiver circuit was tested using the divided master clock provided by the transmitter circuit. Figure 8 shows the measured sampling gate intermediate-frequency output power to input signal power ratio. According to the requirements of the measuring principle described above, we found a cut-off frequency of about 6.5 GHz for the sampling gate (see Fig. 8). The measured hold time clearly exceeds 100 ns for most chip samples.

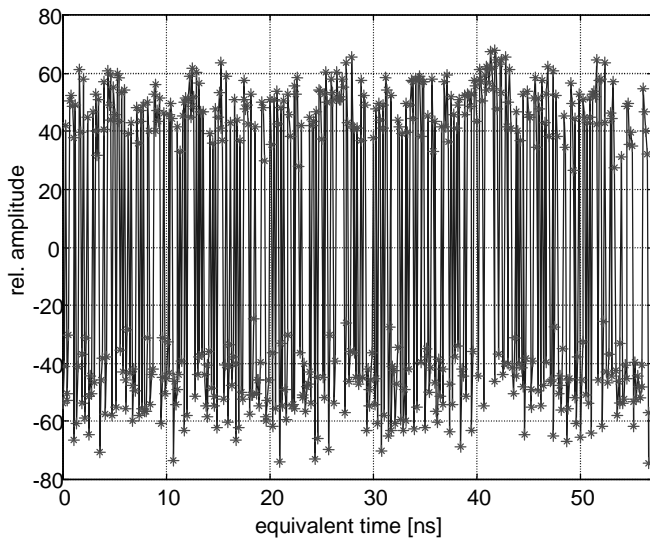


Fig. 9: One period of the sampled and digitised UWB signal at 10 GHz master clock rate

The overall behaviour of the UWB radar head is summarised in Figures 9 and 10. For that purpose the output and input ports were connected by a 10 dB attenuator simulating a frequency independent system. The captured signal clearly shows the random character of the test signal. It was sampled and digitised by a rate of about 20 MHz.

The impulse response of the whole system is demonstrated in Fig. 10. It is determined by the cross correlation

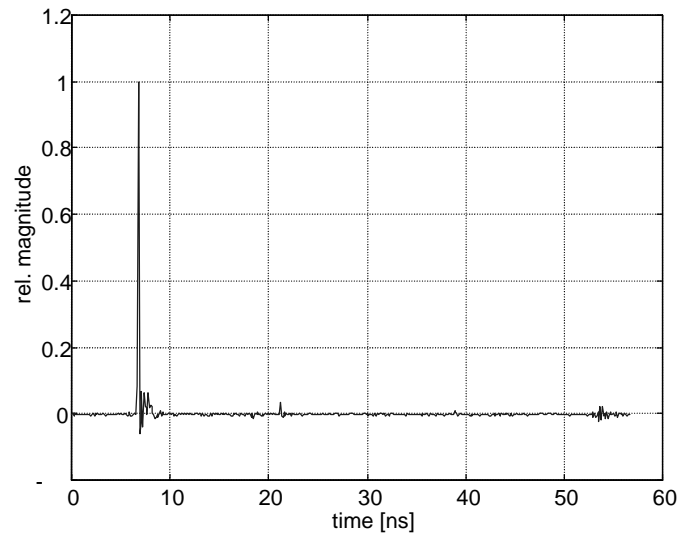


Fig. 10: Impulse response of the UWB head (cross correlation of the measured signal)

function of the measurement signal with a MLBS. No correction was made to suppress the spurious within the pulse base, which are caused by non-linear effects. The time scale in both figures is referred to the stimulation and not to the acquisition domain.

Conclusion

The SiGe HBT technology is useful for realisation of integrated circuits working at high frequencies. In this paper we demonstrated transmitter and receiver integrated circuits operating at 11 GHz. These circuits are used in a new ultra wideband radar system.

Acknowledgement

The authors thank the technology team of the IHP for fabrication of the SiGe HBT integrated circuits.

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